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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,715	07/27/2001	Chi-Lie Wang	3COM 3715-1	8232

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EXAMINER	
CHANG, RICHARD	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,715	WANG ET AL.	
	Examiner	Art Unit	
	Richard Chang	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-17,21-33 and 37-48* is/are rejected.

7)☒ Claim(s) *2-4,18-20 and 34-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment and Arguments

1. Applicant's Amendment and arguments, filed on 08/03/2006, with respect to claims 1-48 have been considered but are moot in view of the new ground of rejection.

In response to applicant's argument that Bass et al. did not disclose nor suggest "logic to dynamically allocate space in said memory to the queue in the plurality of queue" (See Applicant ' Amendment A, page 9, 1st and 3rd paragraph and page 10, 1st and 2nd paragraphs), Bass et al. further teach a direct memory access channel arbiter (6 as DMA-ARB) to dynamically allocate space in memory to the queue in the plurality of queue (See Fig. 1, Col. 3, lines 49-59) and a process for scheduling operation to coordinate the Q-allocation state machine (See Fig. 7, Col. 4, lines 23-28), thus Bass Bass et al. fully discloses and suggests the limitation "logic to dynamically allocate space in said memory to the queue in the plurality of queue" in a broad and reasonable interpretation.

It is the examiner's position that it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Bass et al. with Yavatkar et al. to obtain the inventions specified in claims 1, 17 and 33, since Bass et al. fully discloses and suggests the limitation "logic to dynamically allocate space in said memory to the queue in the plurality of queue" in a broad and reasonable interpretation at the time of the invention was made.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 5-17, 21-33 and 37-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,728,265 ("Yavatkar et al.") in view of US patent No. 6,052,375 A ("Bass et al.").

Regarding claims 1, 17 and 33, Yavatkar et al. teach a computer system, peripheral device and method for controlling frame transmission in connection with a network controller (a computer system, IC and method), comprising of:

a host processor (54), and

a network interface (52) coupled to the host processor (54) and to a network (53) (See Fig. 4, Col. 3, lines 3-7), the network interface (52) comprising:

a first port (72 as PCI bus port) that receives data from the host processor (54),

a second port (52 as network control port) that transmits data to the network (53),

a memory (122) that stores data packets received by the PCI bus port (72 as first port), the memory being coupled to the PCI bus port (72 as first port) and to the a network control port (90 as second port) (See Fig. 5, Col. 5, lines 21-30),

a control circuit (400 as scheduler) that manages the memory as a plurality of queues having respective priorities (402,404), including logic to place a packet received from the host into one of the plurality of queues according to a quality of service

parameter associated with the packet, and logic to service packets in the plurality of queues according to the respective priorities (See Fig. 5A, Col. 6, lines 18-32), and

logic (inside 52) to dynamically allocate space in said memory (queue memory) to the queues in the plurality of queues (See Fig. 7, Col. 7, lines 1-18).

Yavatkar et al. teaches substantially all the claimed invention but did not disclose expressly in further details of the particular application involving limitations of

"a memory that stores data packets received by input port, the memory being coupled to the first port and to output port" and "logic to dynamically allocate space in said memory to the queues in the plurality of queues".

Bass et al. teaches a method for the shaping and scaling of internetworking traffic in high-speed network devices that is common to have a memory (Q0..Q31 as queue memory) that it store data packets received by first port (input port) to the memory being coupled to input port and to output port and logic to dynamically allocate space in memory to the queues in the plurality of queues (2 traffic queue allocation manager) (See Fig. 1, Col. 3, lines 49-67) and a direct memory access channel arbiter (6 as DMA-ARB) to dynamically allocate space in memory to the queue in the plurality of queue (See Fig. 1, Col. 3, lines 49-59) and a process for scheduling operation to coordinate the Q-allocation state machine (See Fig. 7, Col. 4, lines 23-28).

A person of ordinary skill in the art would have been motivated to employ Bass et al. in Yavatkar et al. in order to obtain a computer system, peripheral device and method for controlling frame transmission in connection with a network controller and to take advantage of having a queue memory coupled to input port and to output port to

store data packets received by input port and a direct memory access channel arbiter to dynamically allocate space in memory to the queue in the plurality of queue and a process for scheduling operation to coordinate the Q-allocation state machine in claims 1, 17 and 33.

The suggestion/motivation to do so would have been to have a queue memory coupled to input port and to output port to store data packets received by input port and a direct memory access channel arbiter to dynamically allocate space in memory to the queue in the plurality of queue and a process for scheduling operation to coordinate the Q-allocation state machine, as suggested by Bass et al. in Col. 3, lines 49-67 and Col. 4, lines 23-28. At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Bass et al. with Yavatkar et al. to obtain the inventions specified in claims 1, 17 and 33.

Regarding claims 5, 21 and 37, as discussed above, these claims have limitations that is similar to those of claims 1, 17 and 33 and Yavatkar et al. further teach the processing of security field 150 for security/authentication attributes of the packet (See Fig. 6, Col. 3, lines 38-52), thus it is rejected with the same rationale applied against claims 1, 17 and 33 above, thus it is rejected with the same rationale applied against claims 1, 17 and 33 above.

Regarding claims 6, 22 and 38, as discussed above, these claims have limitations that is similar to those of claims 1, 17 and 33 and Yavatkar et al. further teach that a network controller (52 at the second port) further comprises circuitry for formatting packets according to a protocol compliant with a local area network (LAN) controller (an

Ethernet protocol standard) (See Fig. 4, Col. 3, lines 3-7), thus it is rejected with the same rationale applied against claims 1, 17 and 33 above.

Regarding claims 7, 23 and 39, as discussed above, these claims have limitations that is similar to those of claims 1, 17 and 33 and Yavatkar et al. further teach that a network control port (52 as second port) supports high bandwidth protocol (InfiniBand protocol standard) (See Fig. 5, Col. 5, lines 21-30), thus it is rejected with the same rationale applied against claims 1, 17 and 33 above.

Regarding claims 8, 24 and 40, as discussed above, these claims have limitations that is similar to those of claims 1, 17 and 33 and Yavatkar et al. further teach that a network control port (52 as second port) supports a Transmission Control Protocol/Internet Protocol (TCP/IP), inherently supports the quality of service parameters comprised in the codes of frame start headers. (See Fig. 4, Col. 3, lines 9-15), thus it is rejected with the same rationale applied against claims 1, 17 and 33 above.

Regarding claims 9, 25 and 41, as discussed above, these claims have limitations that is similar to those of claims 1, 17 and 33 and Yavatkar et al. further teach that a driver program (57 said logic to dynamically allocate space in said memory 100) may be stored flow tuples (140) in the memory (100) (maintains a list of used buffers) and may remove existing flow tuples (140) from the memory (100) (maintains a list of free buffers) for each of the plurality of queues (See Fig. 4 ad 6, Col. 3, lines 56-62), thus it is rejected with the same rationale applied against claims 1, 17 and 33 above.

Regarding claims 10-11, 26-27 and 42-43, as discussed above, these claims have limitations that is similar to those of claims 1, 17 and 33 and Yavatkar et al. further that a driver program (57 said logic to dynamically allocate space) downloads packets to a plurality of buffers (140's in non-contiguous memory location) in a single storage array (said memory 100) (See Fig. 4, Col. 3, lines 3-7), thus it is rejected with the same rationale applied against claims 1, 17 and 33 above.

Regarding claims 12-13, 28-29 and 44-45, as discussed above, these claims have limitations that is similar to those of claims 1, 17 and 33 and Yavatkar et al. further that a driver program (57 said logic to dynamically allocate space in said memory 100) maintains a list of free buffers and a list of used buffers for each of the plurality of queues, so that each virtual path has a free buffer list having a number of free buffers, and includes logic which releases a used buffer to the free buffer list for a queue in the plurality of queues having a lowest priority (402 smallest number of free buffers) or a highest priority (404 largest amount of traffic) (See Fig. 5A, Col. 6, lines 31-50), thus it is rejected with the same rationale applied against claims 1, 17 and 33 above.

Regarding claims 14-15, 30-31 and 46-47, as discussed above, these claims have limitations that is similar to those of claims 1, 17 and 33 and Yavatkar et al. further that an emulated direct memory access (DMA) channels transfers the data into the appropriate buffer (304), inherently maintains a list of buffer descriptor for corresponding buffers in said memory (100), including a variable (programmable parameter) specifying a size of the corresponding buffer, and a location of the corresponding buffer (See Fig.

5, Col. 5, lines 29-41), thus it is rejected with the same rationale applied against claims 1, 17 and 33 above.

Regarding claims 16, 32 and 48, as discussed above, these claims have limitations that is similar to those of claims 1, 17 and 33 and Yavatkar et al. further teach that one or more FIFO memories (106) (at least one queue ... FIFO queue) through the data path (92) (See Fig. 5, Col. 5, lines 21-24), thus it is rejected with the same rationale applied against claims 1, 17 and 33 above.

Allowable Subject Matter

4. Claims 2-4,18-20 and 34-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if no art rejection can be applied.

Reason for indicating Allowable Subject Matter

5. The following is an examiner's statement of reasons for allowance:

The prior art along or in combination fails to teach or make obvious the limitations that specifically comprises:

"including a timeout timer coupled with the lower priority queue which is enabled if a packet is stored in the lower priority queue and expires after a timeout interval, and including logic to preempt the higher priority queue in favor of the lower priority queue if the timeout timer expires" as recited in the *dependent claims 2, 18 and 34,*

"a first timeout timer coupled with the intermediate priority queue which is enabled if a packet is stored in the intermediate priority queue and expires after a first timeout interval, and including logic to preempt the higher priority queue in favor of the intermediate priority queue if the first timeout timer expires; and a second timeout timer coupled with the lower priority queue which is enabled if a packet is stored in the lower priority queue and expires after a second timeout interval, and including logic to preempt the higher priority queue and the intermediate priority queue in favor of the lower priority queue if the second timeout timer expires." as recited in the *dependent claims 3, 19 and 35,*

"an first timeout timer coupled with the intermediate priority queue which is enabled if a packet is stored in the intermediate priority queue and expires after a first timeout interval, and including logic to preempt the higher priority queue in favor of the intermediate priority queue if the first timeout timer expires;
a second timeout timer coupled with the lower priority queue which is enabled if a packet is stored in the lower priority queue and expires after a second timeout interval, and including logic to preempt the higher priority queue and the intermediate priority queue in favor of the lower priority queue if the second timeout timer expires, and logic to service the intermediate priority queue in favor of the lower priority queue if both the first and second timeout timers expire." as recited in the *dependent claims 4, 20 and 36.*

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Chang whose telephone number is (571) 272-3129. The examiner can normally be reached on Monday - Friday from 8 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

rkc

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